IN THE CLAIMS:

1. (Currently Amended): A bus ~~design~~ apparatus, comprising:

a clock driver;

a clock receiver coupled to the clock driver by two clock bus lines carrying complementary clock pulses;

a plurality of drivers;

a plurality of receivers each coupled to a respective one of the plurality of drivers by data bus lines, said receivers detecting signals on respective data bus lines with respect to a reference voltage derived from a combination of the complementary clock pulses,

wherein said reference voltage is derived from a resistive connection between said complementary clock pulses; and

wherein each of the two clock bus lines is coupled to a supply voltage and ground through a clock bus divider resistor pair.

2. (Currently Amended): The bus as recited in claim 1, wherein ~~said reference voltage is derived from a resistive connection between said complementary clock pulses~~ each of the plurality of bus lines is coupled to a supply voltage and ground through a data bus divider resistor pair.

3. (Currently Amended): The bus as recited in claim [[2]] 1, wherein ~~the resistors~~ a first resistor and a second resistor in the resistive connection have an approximately equivalent resistance.

4. (Original): The bus as recited in claim 3, wherein the resistance is approximately equivalent to the resistance of the bus lines.

5. (Currently Amended): [[The]] A bus ~~as recited in claim 2~~ apparatus, ~~further~~ comprising:

a clock driver;

a clock receiver coupled to the clock driver by two clock bus lines carrying complementary clock pulses;

a plurality of drivers;

a plurality of receivers each coupled to a respective one of the plurality of drivers by data bus lines, said receivers detecting signals on respective data bus lines with respect to a reference voltage derived from a combination of the complementary clock pulses, wherein said reference voltage is derived from a resistive connection between said complementary clock pulses; and

a first filter capacitor connecting said reference voltage signal to ground.

6. (Original): The bus as recited in claim 5, further comprising:

a second filter capacitor connecting said reference voltage to a supply voltage source.

7. (Original): The bus as recited in claim 6, wherein the first and second filter capacitors have an approximately equivalent capacitance.

8. (Original): The bus as recited in claim 7, wherein the capacitance is within a range of approximately 100 pico-farads and approximately 200 pico-farads.

9. (Original): The bus as recited in claim 1, further comprising:

a plurality of outputs from the data receivers coupled to a deskew/retiming logic component.

10. (Currently Amended): A data processing system, comprising:

a plurality of components; and

a bus coupling at least two of the plurality of components; wherein the bus comprises:

a clock driver;

a clock receiver coupled to the clock driver by two clock bus lines carrying complementary clock pulses;

a plurality of drivers;

a plurality of receivers each coupled to a respective one of the plurality of drivers by data bus lines, said receivers detecting signals on respective data bus lines with respect to a reference voltage derived from a combination of the complementary clock pulses,

wherein said reference voltage is derived from a resistive connection between said complementary clock pulses; and

wherein each of the two clock bus lines is coupled to a supply voltage and ground through a clock bus divider resistor pair.

11. (Currently Amended): The data processing system as recited in claim 10, wherein ~~said reference voltage is derived from a resistive connection between said complementary clock pulses~~ each of the plurality of bus lines is coupled to a supply voltage and ground through a data bus divider resistor pair.

12. (Currently Amended): The data processing system as recited in claim [[11]] 10, wherein ~~the resistors~~ a first resistor and a second resistor in the resistive connection have an approximately equivalent resistance.

13. (Original): The data processing system as recited in claim 12, wherein the resistance is approximately fifty ohms.

14. (Currently Amended): [[The]] A data processing system ~~as recited in claim 11~~, ~~further~~ comprising:

a plurality of components; and

a bus coupling at least two of the plurality of components; wherein the bus comprises:

a clock driver;

a clock receiver coupled to the clock driver by two clock bus lines carrying complementary clock pulses;

a plurality of drivers;

a plurality of receivers each coupled to a respective one of the plurality of drivers by bus lines, said receivers detecting signals on respective bus lines with respect to a reference voltage derived from a combination of the complementary clock pulses, wherein said reference voltage is derived from a resistive connection between said complementary clock pulses; and

a first filter capacitor connecting said reference voltage signal to ground.

15. (Original): The data processing system as recited in claim 14, further comprising:

a second filter capacitor connecting said reference voltage to a supply voltage source.

16. (Original): The data processing system as recited in claim 15, wherein the first and second filter capacitors have an approximately equivalent capacitance.

17. (Original): The data processing system as recited in claim 16, wherein the capacitance is within a range of approximately 100 pico-farads and approximately 200 pico-farads.

18. (Currently Amended): The data processing system as recited in claim [[11]] 10, further comprising:

a plurality of outputs from the data receivers coupled to a deskew/retiming logic component.

19. (New): The bus apparatus as recited in claim 1, wherein a first resistor and a second resistor in the clock bus divider resistor pair have an approximately equivalent resistance.

20. (New): The bus apparatus as recited in claim 19, wherein the first resistor and the second resistor in the data bus divider resistor pair have a resistance that is approximately equivalent to a resistance of the clock bus lines.

21. (New): The bus apparatus as recited in claim 2, wherein a first resistor and a second resistor in the data bus divider resistor pair have an approximately equivalent resistance.

22. (New): The bus apparatus as recited in claim 21, wherein a first resistor and a second resistor in the data bus divider resistor pair have a resistance that is approximately equivalent to a resistance of the data bus lines.

23. (New): The bus as recited in claim 5, wherein a first resistor and a second resistor in the resistive connection have an approximately equivalent resistance.

24. (New): The bus as recited in claim 23, wherein the resistance is approximately equivalent to the resistance of the bus lines.